REMARKS

Claims 1-37 were pending at the time of the Office Action. Claims 2, 12, 22, 25, and 28 are cancelled without prejudice in this response. Claims 1, 4, 5, 11, 14, 15, 21, 24, 27, and 30 are amended. No new matter is added. Claims 1, 3-11, 13-21, 23, 24, 26, 27, 29, and 30-37 are pending at this time. Claims 1, 11, 21, 24, 27, and 30 are independent claims. Reconsideration and allowance of the above-referenced application are respectfully requested.

Specification

The Specification is objected to. Amendments to the Specification obviate these objections.

The Office Action describes that the Specification does not disclose "a computer program product," "a machine-readable medium," or "a computer program product, tangibly embodied in a machine-readable medium." *See, e.g., Office Action,* page 2, last paragraph – page 3, 1st paragraph. As amended, the Specification recites "The operations can be implemented in a computer program product, tangibly embodied in an information carrier that does not include a propagated signal, e.g., a machine-readable medium. The computer program product is operable to cause a machine to perform the operations described previously." Applicants respectfully submit that this recitation is not new matter.

The MPEP states:

> Where subject matter not shown in the drawing or described in the description is claimed in the application as filed, and such original claim itself constitutes a clear disclosure of this subject matter, then the claim should be treated on its merits, and requirement made to amend the drawing and description to show this subject matter.

See, MPEP §608.01(l).

As set forth in the MPEP, subject matter claimed in the application as filed constitutes a clear disclosure of this subject matter.

The recitation "computer program product, tangibly embodied in an information carrier" is included in the preamble of claim 11 in the application as filed. Because the

preamble of claim 11 is part of an original claim, the recitations, "computer program product" and "information carrier," constitute a clear disclosure of this subject matter. Therefore, adding "a computer program product" and "an information carrier" to the Specification does not amount to adding new matter.

Further, the MPEP states:

> While an applicant is not limited to the nomenclature used in the application as filed, he or she should make appropriate amendment of the specification whenever this nomenclature is departed from by amendment of the claims so as to have clear support or antecedent basis in the specification for the new terms appearing in the claims. This is necessary in order to insure certainty in construing the claims in the light of the specification, *Ex parte Kotler*, 1901 C.D. 62, 95 O.G. 2684 (Comm'r Pat. 1901).

See, MPEP, §608.01(o)

Thus, as described in the MPEP, amendment to the specification should be made so as to have clear support in the Specification for new terms appearing in the claims. In order to have clear support in the Specification for the term "machine-readable medium," the Specification is amended to recite "an information carrier that does not include a propagated signal, e.g., a machine-readable medium." At least for this reason, this recitation does not amount to new matter.

Furthermore, during prosecution, the Office objected to the recitation "information carrier." *See, e.g., Office Action* mailed on December 23, 2005. In response, claim 11 was amended to instead of "information carrier" and to recite "machine-readable medium" instead. The Specification does not explicitly recite "machine-readable medium." Several examples of media, e.g., hard drive, RAM, ROM, SRAM, DRAM, are disclosed in the Specification. *See, e.g., Specification,* page 3, lines 19 – 23. One skilled in the art will readily recognize that the examples described in the Specification are information carriers and that such media are machine-readable. Thus, "machine-readable medium" is not new matter.

35 U.S.C. §102 & 35 U.S.C. 103

Claims 1, 9-11, 19-21, 24, 27, 30, and 33-37 stand rejected under 35 U.S.C. §102(e) as being anticipated by Calvignac et al. (US 2003/0048785), hereinafter

"Calvignac." Claims 3, 6-8, 13, 16-18, 23, 26, 29, and 32 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Calvignac in view of Kloth et al. (US 6,570,877), hereinafter "Kloth." Claims 2, 4, 5, 12, 14, 15, 22, 25, 28, and 31 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Calvignac in view of Dice et al. (US 2003/0229766), hereinafter "Dice." The cancellation of claims 2, 12, 22, 25, and 28 obviate the rejections of these claims. Amendments to claims, as listed above, obviate the rejections of the pending claims.

Calvignac does not describe or suggest all the features of claim 1. Calvignac teaches a method and system for identifying a data structure associated with a packet of data. *See, e.g., Calvignac* at Abstract. Calvignac describes a processor internal to a packet processor that may extract one or more fields in a packet header field of a received packet of data to generate a search key. *Id.* Calvignac's internal processor may then be configured to select which table, e.g., routing table, quality of service table, filter table, needs to be accessed using the search key in order to process the received packet of data. *Id.* A determination may then be made by the internal processor as to whether a CAM or a hash table and a Patricia Tree are used to identify the data structure associated with the received packet of data. *Id.* Based on table definitions in a register, the internal processor may make such a determination. *Id.*

The Office contends that Calvignac teaches the claimed multithreaded engine. *See, e.g., Office Action,* page 4, 1st paragraph. Specifically, the Office contends that Calvignac's packet processor 103 is the claimed multithreaded engine. *Id.* Applicants respectfully disagree. Calvignac's packet processor is configured to receive packets, i.e., frames of data from switch fabric 101 and transmit the packets, i.e., frames of data to another switch 100 in the packet switching network. *See, e.g., Calvignac*, paragraph 0020. Calvignac does not describe or suggest that the packet processor is a multithreaded engine, as claimed. In fact, no portion of Calvignac describes or suggests a multithreaded engine. Because Calvignac does not describe or suggest the claimed multithreaded engine, Calvignac certainly does not teach the claimed memory device that is included in the multithreaded engine or the claimed executable instructions stored in the multithreaded engine.

Further, the Office concedes that Calvignac does not teach maintaining a count of a number of threads included in the multithreaded engine that use the memory entry when the multithreaded engine executes the executable instructions. *See, e.g., Office Action,* page 9, 6th paragraph. The Office relies on Dice to teach this feature. In this regard, the Office Action states "Dice discloses maintaining a count of threads that use the memory entry." *Id.* at 8th paragraph. Applicants respectfully disagree. Dice does not teach the claimed count of a number of threads.

Dice teaches mechanisms and techniques to perform a memory management technique such as garbage collection. *See, e.g., Dice* at Abstract. The cited portion of Dice teaches a root array reference structure that can be used if the memory management technique implements a moving or copying garbage collection technique. *See, e.g., Dice*, paragraph 0097. Dice's root array contains entries 188-1 to 188-N that appear as {reference, Reference-Count}. *Id.* Dice's Reference-Count field indicates how many stack cells 160-1 through 160-N point to the root array entry 188. *Id.* Thus, Dice's Reference-Count is not a count of a number of threads included in a multithreaded engine. In fact, Dice does not describe or suggest a multithreaded engine.

Thus, neither Calvignac nor Dice, taken alone or in any combination describe or suggest the claimed multithreaded engine or the claimed count of a number of threads included in the multithreaded engine. Therefore, a *prima facie* case of obviousness is not established. Accordingly, claim 1 is patentable. Kloth does not rectify the deficiencies of Calvignac or Dice. Accordingly, all claims dependent from claim 1 are also patentable at least for reasons similar to claim 1 and for the additional recitations that they contain.

Claim 11, its dependents, claim 27, and its dependents are also patentable at least for similar reasons and for the additional recitations that they contain.

As amended, claim 21 recites "allocate a memory entry in a memory device included in a multithreaded engine to executable instructions stored in the multithreaded engine, the executable instructions to be executed on the multithreaded engine included in a packet processor; include a unique identifier assigned to the executable instructions in a portion of the memory entry; maintain a count of a number of threads included in

the multithreaded engine that use the memory entry when the multithreaded engine executes the executable instructions; determine that the memory entry is no longer being used by a thread included in the multithreaded engine; and decrement the count." (Emphasis added).

Claim 21 is patentable at least for reasons similar to claim 1. In addition, neither Calvignac nor Dice nor Kloth, taken alone or in any combination, describe or suggest the claimed "determine that the memory entry is no longer being used by a thread included in the multithreaded engine; and decrement the count."

Accordingly, claim 21 and all claims dependent therefrom are patentable.

Claim 24 recites "allocate a memory entry in a memory device included in a multithreaded engine to executable instructions stored in the multithreaded engine, the executable instructions to be executed on the multithreaded engine included in a packet processor; include a unique identifier assigned to the executable instructions in a portion of the memory entry; maintain a count of a number of threads included in the multithreaded engine that use the memory entry when the multithreaded engine executes the executable instructions; determine the initiation of use of the memory entry by a thread included in the multithreaded; and in response to the determining, increment the count." (Emphasis added).

Claim 24 is also patentable at least for reasons similar to claim 1. In addition, neither Calvignac nor Dice nor Kloth, taken alone or in any combination, describe or suggest the claimed "determine the initiation of use of the memory entry by a thread included in the multithreaded; and in response to the determining, increment the count."

Accordingly, claim 24 and all claims dependent therefrom are patentable.

Claim 30 recites "allocating a 32-bit long content-addressable-memory (CAM) entry to an executable microblock to be executed on a multithreaded microengine included in a network processor, the 32-bit long CAM entry and the executable microblock located in the multithreaded engine; and including a 4-bit long unique identifier assigned to the executable microblock in a portion of the CAM entry." (Emphasis added).

As described previously, neither Calvignac nor Dice nor Kloth, taken alone or in any combination, describe or suggest a multithreaded engine. Further, the Office

contends that Calvignac teaches the claimed allocating a content-addressable memory (CAM) entry to an executable microblock. *See, e.g., Office Action*, page 5, 4th paragraph. Even if it were assumed that Calvignac's "entry" within "CAM 211" is the claimed "CAM entry," Calvignac does not describe or suggest that the claimed CAM entry is 32 bits long. On the contrary, Calvignac's entry number is 36 bits long. *See, e.g., Calvignac*, paragraph 0031. Furthermore, the Office contends that Calvignac teaches the claimed unique identifier. *See, e.g., Office Action*, page 5, 5th paragraph. Assuming arguendo that Calvignac's "entry number" is the claimed "unique identifier," Calvignac's entry number is not 4 bits long. Calvignac describes that the particular entry number can be manipulated into one or more possible formats that can be either 2 bits (Type Field) or 26 bits (Address) or Next Bit to Test (8 bits). *See, e.g., Calvignac*, paragraph 0030. No portion of Calvignac describes or suggests a 4 bit long unique identifier.

Thus, Calvignac does not describe all the features of claim 30. Accordingly, claim 30 and all claims dependent therefrom are patentable.

CONCLUSION

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the remarks made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

In view of the foregoing amendments and remarks, Applicants respectfully submit that the application is in condition for allowance, and such action is respectfully requested at the Examiner's earliest convenience.

Applicant asks that all claims be allowed. Please apply any credits or charges to deposit account 06-1050.

Respectfully submitted,

Date: October 28, 2008

/ Sushil Shrinivasan L0368 /
Sushil Shrinivasan
Reg. No. L0368

Fish & Richardson P.C.
PTO Customer No.: 20985
12390 El Camino Real
San Diego, California 92130
(858) 678-5070 telephone
(858) 678-5099 facsimile

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